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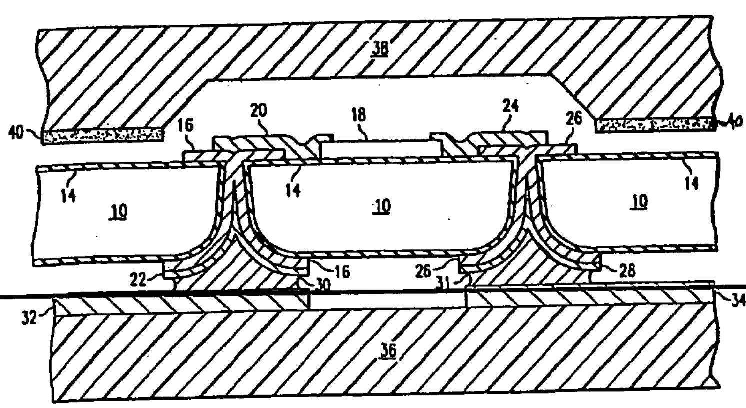
(54) Surface-mounted substrate structure and method

(57) A surface-mounted substrate structure is provided that includes a substrate (10), a doped semiconductor layer (16), and a dielectric layer (14). The substrate (10) has an upper surface and a lower surface and an interconnect opening (12) extending between the upper surface and the lower surface of the substrate (10). The doped semiconductor layer (16) is positioned within the interconnect opening (12). The doped semiconductor layer (16) is also positioned above the upper surface and below the lower surface of the substrate material (10) in an area surrounding the interconnect opening (12). The dielectric layer (14) is positioned between the doped semiconductor layer (16) and the substrate material (10).

FIG. 2



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description, wherein like reference numerals represent like parts or similar areas, in which:

FIGUREs 1A through 1G are a series of schematic cross-sectional diagrams illustrating one embodiment of a surface-mounted substrate structure and method for forming the same;

FIGURE 2 is a schematic cross-sectional diagram illustrating one embodiment of the surface-mounted substrate structure as mounted on a circuit board; and

FIGURE 3 is a schematic cross-sectional diagram illustrating another embodiment of the surface-mounted substrate structure having an insulating protective coating and as mounted on the circuit board.

DETAILED DESCRIPTION OF THE INVENTION

FIGUREs 1A through 1G are a series of schematic cross-sectional diagrams illustrating one embodiment of the fabrication of a surface-mounted substrate structure according to the present invention. Referring to FIGURE 1A, a substrate 10 is provided which may be made of any suitable material. For example, substrate 10 may be provided as a silicon bulk wafer substrate, such as single-crystalline silicon, with a thickness of around twenty to twenty-five mils.

Referring now to FIGURE 1B, an interconnect opening 12 is formed through substrate 10. Interconnect opening 12 may be formed using known or conventional etching techniques such as orientation dependent etch ("ODE") or other suitable methods, such as a laser. Interconnect opening 12 can be formed by starting at a bottom surface of substrate 10 and etching a hole through substrate 10 to an upper surface. In one embodiment, the profile of interconnect opening 12, as illustrated in FIGURE 1B, will present angled walls. The opening of interconnect opening 12 may be greater on the bottom surface than on the upper surface.

Proceeding next to FIGURE 1C, a dielectric layer 14 is grown or deposited on the exposed surfaces of substrate 10. This includes the upper and lower surfaces and the internal surface walls of interconnect opening 12. Dielectric layer 14 may be formed by growing or depositing an oxide using any known or conventional techniques. Dielectric layer 14 may be provided as silicon dioxide if substrate 10 is provided as a silicon substrate.

Referring now to FIGURE 1D, a doped semiconductor layer 16 is deposited on the exposed surface of dielectric layer 14. Doped semiconductor layer 16 may be doped with either p-type dopant, such as boron, to form a p+ layer, or with an n-type dopant, such as phosphorous. In either event, doped semiconductor layer 16 will be provided as either a p-type or an n-type layer and will generally be provided as a doped polysilicon layer that serves as a conductor. Doped semiconductor layer 16 covers the exposed portion of dielectric layer 14 and thus is shown covering the exposed surface of dielectric layer 14 within interconnect opening 12. It should also be noted that interconnect opening 12 will be "pinched" or closed off at the opening near the upper surface of substrate 10. By design, the diameter of interconnect opening 12 and the thickness of doped semiconductor layer 16 are chosen to cause interconnect opening 12 to be sealed. Doped semiconductor layer 16 may be deposited using conventional deposition techniques or any of a variety of deposition techniques such as chemical vapor deposition.

Referring now to FIGURE 1E, portions of doped semiconductor layer 16 are removed through etching. The portions that were removed previously resided on the upper surface of dielectric layer 14 and substrate 10.

Referring now to FIGURE 1F, a device 18 is fabricated or built within the area or region next to the portion of doped semiconductor layer 16 that remains on the surface of dielectric layer 14 and substrate 10. Device 18 may be virtually any device such as a MEMS or IC. Generally, MEMS are fabricated on the surface of substrate 10 and dielectric layer 14 and use these layers for mechanical support. However, ICs generally include doped regions, for example source regions and drain regions for field-effect transistors, that are fabricated into substrate 10. ICs may include any of a variety of individual circuit elements such as transistors, capacitors, resistors, diodes, and virtually any circuit element that may be fabricated within a substrate such as substrate 10. If device 18 is fabricated as an IC, dielectric layer 14 may be patterned and etched away so that device 18 may extend within substrate 10.

Referring finally to FIGURE 1G, a contact metal 22 is provided within the remaining portion of interconnect opening 12 and extends over the exposed surface of doped semiconductor layer 16 that is present within interconnect opening 12 and the bottom of dielectric layer 14 and substrate 10. After contact metal 22 has been deposited onto doped semiconductor layer 16, portions of both contact metal 22 and doped semiconductor layer 16 that reside on either side of interconnect opening 12 are removed using any suitable or conventional etching method. Contact metal 22 is later used for contacting a circuit board interconnect line or a conductor within an IC package.

An interconnect metal 20 is deposited between doped semiconductor layer 16, residing on the upper surface of dielectric layer 14, and device 18. Interconnect metal 20 serves as a conductor between a contact or bonding pad location of device 18 and doped semiconductor layer 16. As illustrated, portions of interconnect metal 20 may reside on the upper surface of doped semiconductor layer 16 and device 18. Thus, by providing interconnect metal 20 as shown in FIGURE 1G, a conductor path is provided between a contact or bonding pad location of device 18 and contact metal 22. Interconnect metal 20 may be virtually any available

example, although the structure has been illustrated and described using conventional semiconductor fabrication techniques, other techniques, whether currently known or not, could potentially be used to fabricate the surface-mounted substrate structure of the present invention. Also, some of the steps described and illustrated in the preferred embodiment as discrete or separate steps may be combined into one step without departing from the scope of the present invention. Other examples of changes, substitutions, and alterations are readily ascertainable by one skilled in the art and could be made without departing from the spirit and scope of the present invention.

Claims

1. A surface-mounted substrate structure comprising:

   a substrate material having an interconnect opening extending between an upper surface and a lower surface thereof;
   a conductive layer positioned within the interconnect opening, the conductive layer also positioned substantially above the upper surface and below the lower surface of the substrate material in an area around at least a portion of the interconnect opening; and
   a dielectric layer positioned substantially between the conductive layer and the substrate material.

2. The structure of Claim 1, wherein the conductive layer comprises a doped semiconductor layer.

3. The structure of Claim 2, wherein the doped semiconductor layer comprises doped polysilicon.

4. The structure of any of Claims 1 to 3, wherein the substrate material comprises a plurality of interconnect openings.

5. The structure of any of Claims 1 to 4, wherein the substrate material comprises a silicon bulk substrate.

6. The structure of Claim 5, wherein the silicon bulk substrate comprises single-crystalline silicon.

7. The structure of any of Claims 1 to 6, further comprising a microelectronic mechanical system having a bonding pad, the bonding pad positioned adjacent to the interconnect opening on the upper surface of the substrate material.

8. The structure of any of Claims 1 to 7, further comprising an integrated circuit die having bonding pads, the bonding pads positioned adjacent to the interconnect opening on the upper surface of the substrate material.

9. The structure of Claim 7 or Claim 8, further comprising an interconnect conductor positioned to provide an electrical coupling between the bonding pad and the conductive layer.

10. The structure of any of Claims 1 to 9, further comprising a contact metal positioned adjacent to an exposed side of a portion of the conductive layer positioned within the interconnect opening and below the lower surface of the substrate material.

11. The structure of Claim 10, wherein the contact metal is arranged for mounting to a conductor of a circuit board.

12. The structure of Claim 10, wherein the contact metal is arranged for mounting to a conductor of a circuit board through a mounting material.

13. The structure of Claim 10, wherein the contact metal is arranged for mounting to a conductor of a packaging device.

14. The structure of any of Claims 1 to 13, wherein the dielectric layer comprises an oxide layer.

15. A packaged device comprising:

   a substrate material having a plurality of interconnect openings extending between an upper surface and a lower surface thereof;
   a conductive layer positioned within the interconnect openings, the conductive layer positioned substantially above the upper surface and below the lower surface of the substrate material in an area around at least a portion of each of the interconnect openings;
   a dielectric layer positioned substantially between the conductive layer and the substrate material;
   a microelectronic device having a plurality of bonding pads, each of the plurality of bonding pads positioned adjacent to a corresponding interconnect opening and conductive layer on the upper surface of the substrate material;
   a plurality of interconnect conductors, each interconnect conductor positioned to provide an electrical coupling between each bonding pad and a corresponding conductive layer; and
   a cover for encapsulating the microelectronic device.

17. The packaged device of Claim 16, wherein the dielectric layer comprises an oxide layer.

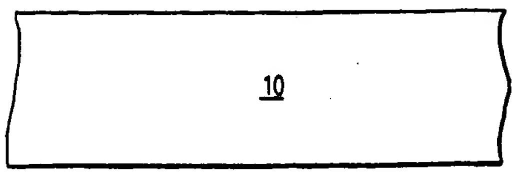

FIG. 1A

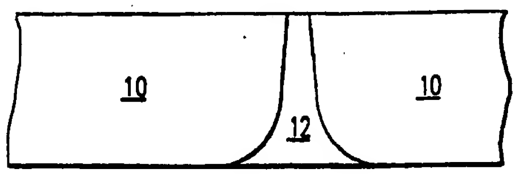

FIG. 1B

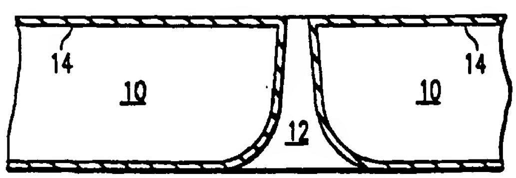

FIG. 1C

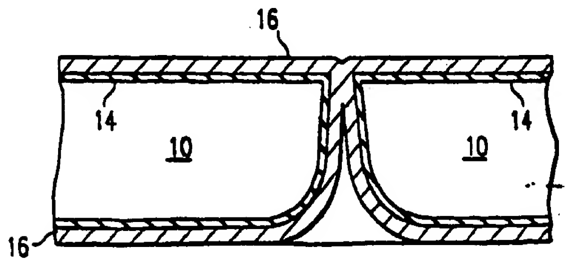

FIG. 1D

FIG. 2